Cadence Design Systems, Inc. (CDNS)

Baird Facts

Please refer to Appendix - Important Disclosures and Analyst Certification.

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</thead>
<tbody>
<tr>
<td>52WK H-L ($) :</td>
<td>87 - 51</td>
<td>L-Term Rev. Gr Rate Est:</td>
<td>Q1</td>
<td>0.54A</td>
<td>0.60A</td>
<td>0.64E</td>
<td></td>
</tr>
<tr>
<td>Market Cap (mil):</td>
<td>24,724</td>
<td>L-Term EPS Gr Rate Est:</td>
<td>Q2</td>
<td>0.57A</td>
<td>0.59E</td>
<td>0.61E</td>
<td></td>
</tr>
<tr>
<td>Shares Out (mil):</td>
<td>280.7</td>
<td>Debt/Cap:</td>
<td>Q3</td>
<td>0.54A</td>
<td>0.65E</td>
<td>0.74E</td>
<td></td>
</tr>
<tr>
<td>Float (mil):</td>
<td>275.1</td>
<td>ROE:</td>
<td>Q4</td>
<td>0.54A</td>
<td>0.69E</td>
<td>0.72E</td>
<td></td>
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<tr>
<td>Avg. Daily Vol (mil):</td>
<td>2.65</td>
<td></td>
<td>Total</td>
<td>2.20A</td>
<td>2.47E</td>
<td>2.71E</td>
<td></td>
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<tr>
<td>Dividend ($) :</td>
<td>0.00</td>
<td></td>
<td>FY P/E</td>
<td>40.0x</td>
<td>35.7x</td>
<td>32.5x</td>
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<tr>
<td>Yield (%):</td>
<td>0.0</td>
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<tr>
<th>Headquartered</th>
<th>IPO/Founded</th>
<th>Dec</th>
<th>2019A</th>
<th>2020E</th>
<th>2021E</th>
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<tr>
<td>San Jose, CA</td>
<td>1987/1982</td>
<td>Revenue (Mil)</td>
<td>2,336.3</td>
<td>2,552.6</td>
<td>2,796.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>% Growth</td>
<td>9.3%</td>
<td>9.3%</td>
<td>8.0%</td>
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<tr>
<td></td>
<td></td>
<td>Operating Margin</td>
<td>32.1</td>
<td>32.8</td>
<td>33.3</td>
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<table>
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<tr>
<th>Management</th>
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<tbody>
<tr>
<td>Chief Executive Officer</td>
<td>Lip-Bu Tan</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chief Financial Officer</td>
<td>John Wall</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Investor Relations</td>
<td>Alan Lindstrom</td>
<td></td>
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Company Description

Cadence Design Systems, Inc., headquartered in San Jose, California, provides software for the design and analysis of integrated circuits (“chips”) and electronic systems. The rapid pace of innovation in the semiconductor industry – achieving higher performance and lower power consumption on smaller chip area – is necessitating greater levels of spending on design and verification and the use of Cadence products. Furthermore, with the importance of software in a modern chip environment, new approaches are required to run, test, and debug software earlier in the development process and often before the silicon is ready; the company offers a portfolio of emulation and prototyping systems that enable this improved workflow. Lastly, Cadence has taken its core competency in computational software for electronic design automation (EDA) and leveraged it into near-term adjacencies targeting system analysis, including simulation and embedded security.

Revenue Profile

Source: Baird estimates, Factset, Company reports

Joe Vruwink, CFA
Sr. Research Analyst
jvruwink@rbaird.com
414.298.5934
Competition
The company competes most frequently with Synopsys and Mentor Graphics (now a part of Siemens AG). Other companies with EDA or electronics design capability include Altium, Ansys, CEVA, Keysight Technologies and Zuken Ltd.

Quick Summary
- Reiterate Outperform rating. Cadence delivered a solid F1Q20 report with EPS of $0.60 vs. $0.54 (+10% YoY) topping our estimate by 6%/consensus by 10%. Favorably, FY20 guidance was reaffirmed though the sequence is a bit different than anticipated with F2Q below consensus expectations (assuming impacts from “shelter-in-place” orders) followed by a strong 2H20 (implying 3-4% upside to consensus expectations). Management has seen no slowdown in design activity, we believe this favorable dynamic should continue to attract incremental investor interest. Raised price target to $91 on higher estimates/valuation methodology.
- Reiterate Outperform rating – we remain buyers.
  - Cadence is a top idea in our coverage. We believe resiliency in customer design activity and several new growth drivers (EDA/ IP products, secular growth from 5G/Al/hyperscale/auto/IoT) strongly position company and stock. Our price target rises to $91 as we increase estimates while assuming 30x our NTM FCF estimate, one year from now.
  - Cadence’s stock performed well into this earnings report, and after-hours trading indicated shares were slightly lower (down <1%). To the extent the stock opens lower, we believe the pullback represents an attractive opportunity.
- F2Q outlook closer to our expectations, below consensus estimates.
  - Our previous estimate revisions assumed a 400-500bp growth impact for Cadence during F2Q in anticipation of potential headwinds on sources of up-front revenue (hardware and IP deliveries).
  - For F2Q, Cadence anticipates revenues of $580-600 million (flat to up 3% YoY) which captures our $593 million estimate but is 500bp below consensus. Management indicated that the low end of guidance assumes “shelter-in-place” orders postpone delivery of hardware and IP products into the second half, whereas the high end assumes delivery commencing sometime in the May time frame.
  - Anticipated EPS of $0.50-0.54 (down 5-12% YoY) reflects a wider variance to our estimate and consensus of $0.57/0.59 respectively. Management noted the forecast is “more conservative than usual” while also assuming dilutive impacts from M&A and the impact of sequentially-lower revenue.
- Pleasant surprise: Fiscal 2020 outlook maintained.
  - Cadence anticipates a strong second half, aided by customer design activity (“seeing no slowdown in activity”). Guidance implies second-half revenue growth of 15% YoY (or 12% excl. extra week in F4Q) with EPS growth of 23% YoY; this is 3-4% better than current consensus and 8% better than our estimates (which assumed COVID-19 impacts lingering into F3Q).
  - A few additional details: 1) backlog of $3.7 billion up 3% sequentially (a strong seasonal performance) and 32% YoY; this is 3-5% better than current consensus and 8% better than our estimates (which assumed COVID-19 impacts lingering into F3Q).
  - China revenues contributed 400bp of growth in F1Q but this likely moderates in coming quarters; 3) while customer base is primarily large entities (top 40 customers = 55-60% of revenue), guidance does contemplate a degree of credit deterioration with smaller customers; and 4) FCF guidance bumped higher (up 10% YoY) with 50% expected to be used for share repurchases.

Investment Thesis
Core EDA business supported by cyclical/secular tailwinds. While many of Cadence’s newer market efforts extend beyond the semiconductor industry, the business today is still predominantly represented by semiconductor companies (approximately 60% of revenues) and EDA tools. In the near term, this exposure is likely to be a positive for the company with semiconductor R&D budgets poised to inflect higher following a more muted year for growth during 2019.

In addition to the potential uptick in market growth, Cadence has introduced numerous new products in the area of digital and custom design that should help to solidify/grow its competitive position. We believe there are three key areas that can continue to enable high-single-digit growth.

- Strengthening the core analog business with new capabilities within the Virtuoso custom design platform, particularly in advanced nodes (e.g., FinFETs) and shortening design/verification cycles.
- Expanding digital presence with full digital flow capabilities across Genus (synthesis), Innovus (place & route), Tempus and Pegasus (sign off) solutions. Unifying the design workflow, versus utilizing point solutions from different vendors, can drive a 10-20% improvement in “power, performance and area” results and quicker turnaround times.
- Exploring cloud opportunities among customers that can benefit from improved scalability, performance, and flexibility. As of October 2019, Cadence cited over 50 customers using the Cadence Cloud platform to some degree.

Verification tools helping to accelerate chip development. Verification products ensure hardware designs perform as intended while enabling earlier software development and debugging before the physical chip is ready. The Cadence Verification portfolio has delivered consistent high-single-digit growth this cycle as customers employ tools accelerate chip development.

Targeted growth in IP likely helps to sustain strong performance. The ongoing push to accelerate time to market and optimize development resources has been a positive secular driver of the intellectual property market, where semiconductor companies are able to utilize pre-designed and pre-verified circuits in the buildout of new chips.

- After undertaking a shift in strategy during 2016 to focus on design IP with high re-use opportunities (versus heavily customized IP for customers), the Cadence IP business has outpaced growth in the broader IP industry – delivering a 17% CAGR versus the IP industry at ~10% – while helping to add approximately 100bp to Cadence’s corporate growth profile.

TAM expansion beyond traditional EDA could drive revenue upside. Cadence is targeting growth outside of the $10 billion EDA market by leveraging its core technical capabilities to pursue system-level solutions for hardware/software integration and system analysis. Two areas in particular – simulation and embedded security – could yield upside to currently forecasted revenue performance.
as new products and technical collaborations become established and gain market traction. Each area individually is a multi-billion-dollar TAM opportunity that has grown at a double-digit rate this cycle, and when combined with an EDA market expected to grow high single digits, underpins the company’s TAM expansion strategy over the next 5-10 years.

**Maintaining “rule of 40” philosophy should yield profitable growth.** Cadence has employed a disciplined investment strategy where R&D spending is poised to increase slightly. The Top 25 largest semiconductor companies (excl. Memory) will see revenues decline by nearly 10% in 2019, yet R&D or product architectures which continue to receive incremental spending, even amid lower industry revenues. As one example, we estimate the Top 25 largest semiconductor companies (excl. Memory) will see revenues decline by nearly 10% in 2019, yet R&D spending is poised to increase slightly.

**Competition.** The company competes most frequently with Synopsys and Mentor Graphics (now a part of Siemens AG). Other companies with EDA or electronics design capability include Altium, Ansys, CEVA, Keysight Technologies and Zuken Ltd.

**Impacts from operating a global business.** Revenue from international operations has approximated 60% of total sales during recent years. Most of the company’s revenues are denominated in U.S. dollar while approximately 30% of total costs and expenses are transacted in foreign currencies. The mismatch between US dollar-denominated revenues and foreign operating expenses can lead to variability in reported transactional gains/losses and resulting profitability.

**Risks.** Key risks include the following: 1) growth in R&D spending by the semiconductor industry and impacts on EDA/IP spending; 2) competition from large global EDA vendors (Synopsys and Mentor Graphics) and companies in the emerging business opportunities of simulation and embedded security; 3) impacts from operating a global business, including foreign currency fluctuation, IP protection, and trade policy uncertainty; 4) timing and magnitude of investments to support growth; 5) impacts from acquisitions, both by the company and among customers (where consolidation can influence spending decisions on EDA tools); 6) modeling risk, particularly around the timing of IP and hardware usage by customers and resulting revenue recognition; and 7) seasonal characteristics of financial and stock performance.

**Risks & Caveats**

**Growth in semiconductor R&D and impacts on EDA/IP spending.** Spending on EDA tools and IP blocks is heavily influenced by new design projects at semiconductor and electronic system companies. These end markets are cyclical and downturns can influence the timing of new projects or size of R&D budgets. One favorable offset in this equation is the introduction of new technology and/or product architectures which continue to receive incremental spending, even amid lower industry revenues. As one example, we estimate the Top 25 largest semiconductor companies (excl. Memory) will see revenues decline by nearly 10% in 2019, yet R&D spending is poised to increase slightly.

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Appendix - Important Disclosures and Analyst Certification

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Rating and Price Target History for: Cadence Design Systems, Inc. (CDNS) as of 05-19-2020

1 Robert W. Baird & Co. Incorporated makes a market in the securities of CDNS.

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